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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,102	12/02/2003	Jens Barrenscheen	INFJR-0005	4397

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EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,102	BARRENSCHEEN ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No._____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/09/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 11 and 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. As per claim 11, it appears unclear regarding the sending of "a transmission clock signal," because claim 11 state that "a transmission clock signal" is transmitted with the diagnostic data (to first semiconductor chip) but also stated that said transmission clock signal is not transmitted to the first semiconductor. Examiner will assume that the diagnostic data are transmitted to the first semiconductor chip based on a clock signal generated within the first semiconductor chip.

4. As per claims 15-16, claims are rejected based on the dependency on claim 11.

5. As per claim 17, it appears unclear if the "transmission clock signal" as stated by the applicant in page 24, lines 13, 15 and 18, is the same or different; and which "transmission clock signal" was transmitted by the second semiconductor chip along with the diagnostic data. Examiner will assume that the "transmission clock signal" is the same and that the second semiconductor chip transmits the diagnostic data in time with the "transmission clock signal" from the first semiconductor chip.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arslain et al. (US Patent 6,366,153) further in view of applicant's admittance as prior art (AAPR).

7. As per claim 1, Arslain teaches a system method comprising a first semiconductor chip (reference number 102, Figure 1) and a second semiconductor chip (reference number 100, Figure 1) connected thereto,

where the second semiconductor chip is additionally connected to an electrical load and drives the electrical load (reference number 118, Figure 1) on the basis of a

serial clock and a serial data (load control data based on timing) (Figure 1; column 2, lines 46-67 and column 3, lines 1-7),

where the first semiconductor chip transmits to the second semiconductor chip the serial clock (SCLK), serial data in (SDI) and chip select (CS) signals (load control data and pilot data) which control the second semiconductor chip (Figure 1; column 2, lines 63-67 and column 3, lines 1-7), and

where the second semiconductor chip transmits to the first semiconductor chip the diagnostic data which represent at least one of the states prevailing in the semiconductor chip and events which occurred in the second semiconductor chip (Figure 1 and column 3, lines 8-50), and

AAPR specifically disclose that the transmission of the load control data and the pilot data from the first semiconductor chip to the second semiconductor chip (reference numbers DATA2, DATA1a, Figure 1); and

the second semiconductor chip includes means for transmitting the diagnostic data via a first transmission channel connected between the first and second semiconductor chips, and the first semiconductor chip includes means for transmitting load control data and obviously the pilot data via a second transmission channel connected between the first and second semiconductor chips (reference number DATA1b, Figure 1).

8. As per claims 2-4, please see clam 1 in view of Arslain and AAPR. Arslain further teaches that the system method further comprising:

wherein the first semiconductor chip is a processor (program controlled unit) (reference number 102, Figure 1 and column 2, lines 51-55);

wherein the second semiconductor chip is a programmable driver (power chip) (reference number 100, Figure 1);

wherein the second transmission channel further comprising:

a SCLK (transmission clock) line via which the first semiconductor chip transmits the SCLK (transmission clock) signal to the second semiconductor chip (Figure 1; column 2, lines 63-67 and column 3, lines 1-7),

a SDI (data) line via which the first semiconductor chip transmits the SDI (load control data and the pilot data) signal to the second semiconductor chip in time with the SCLK (transmission clock) signal (Figure 1; column 2, lines 63-67 and column 3, lines 1-7), and

a CS (chip select) line via which the first semiconductor chip transmits the CS (chip select) signal to the second semiconductor chip (Figure 1; column 2, lines 63-67 and column 3, lines 1-7); and

AAPR further disclose that the chip select (CS) signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the data line ([0023], page 5).

9. As per claim 5, please see clams 1-4 in view of Arslain and AAPR. Arslain further teaches that the first semiconductor chip is coupled to the second semiconductor chip through a serial peripheral interface (SPI), wherein the serial interface have a plurality of control and status registers utilized for communication between the first semiconductor

chip (master) and the second semiconductor chip (slave) (column 2, lines 63-67 and column 3, lines 1-7). Therefore it would be obvious that a plurality of different control and status data are transmitted through the SDI line in units of frames in accordance with the SCLK signal, obviously using a time-division multiplexing scheme to transmit the plurality of different data (control data and pilot data).

10. As per claim 6, please see claims 1-5 in view of Arslain and AAPR. It is obvious that the first semiconductor chip (master), generating the SCLK signal, would define the time windows of constant length and transmit in each time window the plurality of different data (load control data frame or control data frame or no data).

11. As per claim 7, please see claims 1-6 in view of Arslain and AAPR. Arslain further teaches a first temperature register included within the control register of the serial interface and the first temperature register is periodically read and set by the processor (first semiconductor chip), wherein the first temperature register is used to control the PWM signal (column 3, lines 8-34). Therefore, it would be obvious that the first semiconductor chip (master) transmit load control data frame periodically, having a respective length of n time windows between the transmission and no load control data frame is transmitted during this respective length. Further more, it would also be obvious that n can be set to be $n \geq 0$ and that n is set by the processor (user of the arrangement).

12. As per claim 8, please see claims 1-7 in view of Arslain and AAPR. As pilot data and load control data are serially transmitted over the SDI line, it would be obvious that

a pilot data frame can be transmitted only in a time window in which no load control data frame is to be transmitted.

13. As per claim 9, please see claims 1-8 in view of Arslain and AAPR. AAPR further disclose that the pilot data controls the transmission of the load control data ([0009], [0010], pages 2-3);

Therefore, since the pilot data and the load control data are transmitted serially over the SDI line, it would be obvious that the pilot data have a higher priority than the load control data, especially if there is a conflict for transmission between the pilot data and the load control data.

14. As per claim 10, please see clams 1-9 in view of Arslain and AAPR. Arslain further teaches a feedback signal from the over temperature sensing device (OTSD), transfer through the first transmission channel from the second semiconductor chip (slave) to the first semiconductor chip (master) (Figure 1 and column 3, lines 8-33). Therefore, it is obvious that the first transmission channel comprises a data line (for transmitting the feedback signal), and wherein this data line is used to transmit neither load control data nor pilot data.

15. As per claim 11, please see clams 1-10 in view of Arslain and AAPR. It would be obvious that diagnostic data are transmitted in time with the SCLK (transmission clock) signal, wherein the SCLK signal is generated within the first semiconductor chip (master).

16. As per claim 12, please see claims 1-11 in view of Arslain and AAPR. It would have been obvious that the first semiconductor chip (master) transmits appropriate

feedback rate (pilot data) in order to prescribe to the second semiconductor chip (slave) what transmission rate is to be used by the second semiconductor chip (slave) to transmit the diagnostic data to the first semiconductor chip (master).

17. Claims 13-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arslain et al. (US Patent 6,366,153) and AAPR further in view of Hastings et al. (US Patent 6,772,251).

18. As per claim 13, please see claims 1-12 in view of Arslain and AAPR.

Arslain and AAPR fails specifically to teach the transmission rate is prescribed by transmitting a division factor, and wherein the second semiconductor chip (slave) divides the frequency of the SCLK (transmission clock) signal transmitted to it by the first semiconductor chip (master) by the division factor and transmits the diagnostic data to the first semiconductor chip (master) in time with the resultant signal.

Hastings teaches a system method transferring serial data between a master and a slave through a SPI, comprising of a clock divider (reference number 122, Figure 1) at the slave for dividing down the clock frequency from the system clock line and transfer data from the slave to the master using this resulting clock frequency (Figure 1, column 1, lines 29-36, column 2, lines 60-67 and column 3,lines 1-21).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to implement the clock divider in Hastings' master and slave communication system method into Arslain's and AAPR's circuit control system method. Doing so add and further expands Arslain's and AAPR's circuit control system method

by reducing the number of wires needed and reducing the flow of start and stop bits (Hastings, column 1, lines 29-55)

19. As per claim 14, please see claims 1-13 in view of Arslain, AAPR and Hastings. AAPR further discloses the transmission clock signal supplied to the second semiconductor chip (slave) represent the transmission clock, which is used by the first semiconductor chip (master) to transmit the load control data or pilot data signal to the second semiconductor chip (slave) (reference numbers CLK1, CLK2, Data1a, Data2, Figure 1 and [0021]-[0025], page 5).

20. As per claim 15, please see claims 1-14 in view of Arslain, AAPR and Hastings. It is obvious that diagnostic data are transmitted in units of frames; and

Hastings further teaches a frame starting with a start bit having a prescribed value and ends with a stop bit having a prescribed value (reference numbers 310, 318, Figure 3) for serial data transmission.

21. As per claim 16, please see claims 1-15 in view of Arslain, AAPR and Hastings. It would be obvious to oversample the diagnostic data in order for the first semiconductor chip to ascertain the phase of the diagnostic data.

22. As per claim 17, please see clams 1-16 in view of Arslain, AAPR and Hastings. AAPR further discloses that the first transmission channel comprises the transmission clock line via which the first semiconductor chip (master) transmits the transmission clock signal to the second semiconductor chip(slave), and wherein the second semiconductor chip transmits the diagnostic data in time in accordance with the transmission clock signal (reference number CLK1, Data1b, Figure 1).

23. As per claims 18, please see clams 1-17 in view of Arslain, AAPR and Hastings.

AAPR further discloses:

a transmission clock line via which the first semiconductor chip (master) transmits a transmission clock signal to the second semiconductor chip (slave) (reference numbers CLK1, CLK2, Figure 1);

two data line via which the first semiconductor chip (master) transmits the load control data and the pilot data to the second semiconductor chip (slave) in time with the transmission clock signal (reference numbers DATA2, DATA1a, Figure 1); and

a chip select line via which the first semiconductor chip (master) transmits the chip select signal signaling to the second semiconductor chip (slave) the start and end of the transmission of data intended for the second semiconductor chip (slave) via the data line a first data line via which the first semiconductor chip (master) transmits the load control data and the pilot data to the second semiconductor chip (slave) in time with the transmission clock signal (reference numbers CS1, Figure 1).

Therefore, it would have been obvious for the second transmission channel to further comprise:

a first transmission clock line via which the first semiconductor chip (master) transmits a transmission clock signal to the second semiconductor chip (slave);

a second transmission clock line via which the first semiconductor chip (master) transmits the inverse transmission clock signal to the second semiconductor chip (slave),

a first data line via which the first semiconductor chip (master) transmits the load control data and the pilot data to the second semiconductor chip (slave) in time with the transmission clock signal,

a second data line via which the first semiconductor chip (master) transmits the inverse load control data and the inverse pilot data to the second semiconductor chip (slave), and

a chip select line.

24. As per claim 19, please see claims 1-18 in view of Arslain, AAPR and Hastings. Arslain further teaches that the programmable driver is selected base on limiting electromagnetic interference (column1, lines 11-24 and column 5, lines 4-22), therefore it would be obvious that LVDS drivers or other special drivers with limited electromagnetic interference are used for the programmable (output) drivers on the first semiconductor chip (master), which output the SCLK, SDI and CS (load control data, pilot data and transmission clock) signals.

25. As per claim 20, please see claims 1-19 in view of Arslain, AAPR and Hastings. Arslain further teaches that the first semiconductor chip (master) is couple to said single programmable driver (Figure 1), therefore it would have been obvious that the first semiconductor chip (master) is coupled to a plurality of respective different programmable (output) drivers for outputting the SCLK and SDI (load control data, pilot data and transmission clock) signals, and wherein the user of the arrangement is obviously able to set which of the plurality of different programmable (output) drivers needs to be used in each case.

26. As per claim 21, please see claims 1- 20 in view of Arslain, AAPR and Hastings. It would be obvious that the first semiconductor chip (master) is connected to a plurality of second semiconductor chips (slave), and obviously wherein a first portion of the data transmitted in a frame is intended for a first second semiconductor chip (master), and a second portion of the data transmitted in this frame is intended for a second semiconductor chip (slave).

27. As per claim 21, please see claims 1- 21 in view of Arslain, AAPR and Hastings. It would be obvious that every second semiconductor chip is connected to the first semiconductor chip via a dedicated CS (chip select) line;

wherein the CS (chip select) signals are transmitted via the CS (chip select) line; and

Hastings further teaches an enabling (CS) signal used by the slave (reference number 304, Figure 3), wherein the enabling (CS) signal initiates the slave for transmission of data to the master and the enabling (CS) signals can be transmitted (altered) during the transmission of a frame.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671 and email is chun-kuan.lee@uspto.gov. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Popovici Dov can be reached on (571)272-4083. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

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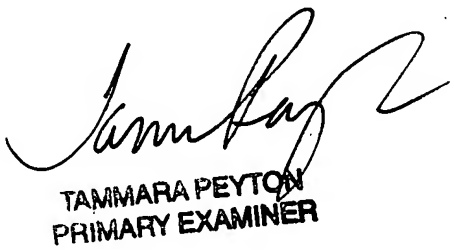

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